REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following remarks is respectfully requested.

Claims 1-20 are presently active in this application with Claims 12 and 20 having been amended by the present Amendment.

In the outstanding Office Action Claim 20 was objected to as including informalities requiring corrections; Claim 13 was rejected under 35 USC §112, 2nd para., as being indefinite; and Claims 1-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sharma (6,910,169), Giles et al. (4,680,760), and further in view of Matsuda et al. (5,509,132).

In response to the objection to Claim 20, the dependency of Claim 20 has been corrected herewith. Likewise, the preamble of Claim 12 has been corrected herewith. Accordingly the grounds for objection/indefiniteness of Claims 20 and 12 are believed to have been overcome.

Applicants respectfully traverse the outstanding rejection on the merits, because in Applicant's view, Claims 1-20 patentably define over the cited prior art.

In particular, pending Claim 1 defines the subject invention as follows:

> 1. A semiconductor integrated circuit comprising:
> a memory;
> an ECC circuit that has an error correction function of N (N is a natural number) bits for output data of the memory; and
> an error detection circuit configured to output a signal indicative of the following fact, if a total of an error bit number n1 detected by the ECC circuit when a first data pattern in testing target addresses of the memory is read out and an error bit number n2 detected by the ECC circuit when a second data pattern that is an inversion of the first data pattern in at least a part of the testing target addresses is read out exceeds N.

As is evident from Claim 1, the claimed invention includes an ECC circuit and an error detection circuit employing inverse data patterns so as to check ECC correction while

simultaneously performing a memory test. It is respectfully submitted that these aspects of Claim 1 are clearly not obviated by the cited prior art, for the reasons next discussed.

The outstanding Office Action relies on a combination of Giles (column 2, line 53; column 4, lines 9-21) and Matsuda et al. (column 9, lines 39-41; column 8, lines 24-29) as suggesting the occurrence of an error is determined when the total of the error bit number corresponding to a first data pattern and the error bit number corresponding to a second data pattern (an inverted pattern) exceeds the predetermined admissible value.

However, whereas Giles may disclose a data pattern and its inverse data pattern, these patterns are not used for evaluating a semiconductor memory. It is therefore believed to be unreasonable hindsight to combine Giles with Matsuda et al. to support a finding of obviousness, where there is not motivation to do so in the references. Indeed, it is respectfully submitted that Giles merely discloses pattern inversion and Matsuda et al. merely discloses a total number of errors. It is respectfully submitted that these teachings stand in isolation, and only are combinable using Applicant's invention as a road map to reconstruct the claimed invention based on hindsight.

Similarly whereas Sharma may disclose error detection using an ECC, nevertheless in the case of a memory having an ECC, a data pattern and its inverse are not generally both used for testing a memory. In contrast, the claimed invention provides a technology for checking ECC correction while simultaneously performing a memory test, such as a march test. Therefore, it is respectfully submitted that the cited references, absent hindsight application of isolated teachings in the references, fail to render obvious the claimed subject matter and that the outstanding rejection on the merits is traversed.

Consequently, in view of the present amendment and in light of the above comments,

it is respectfully submitted that the pending claims are in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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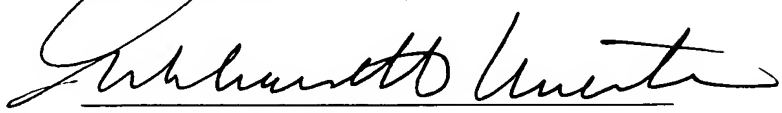

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